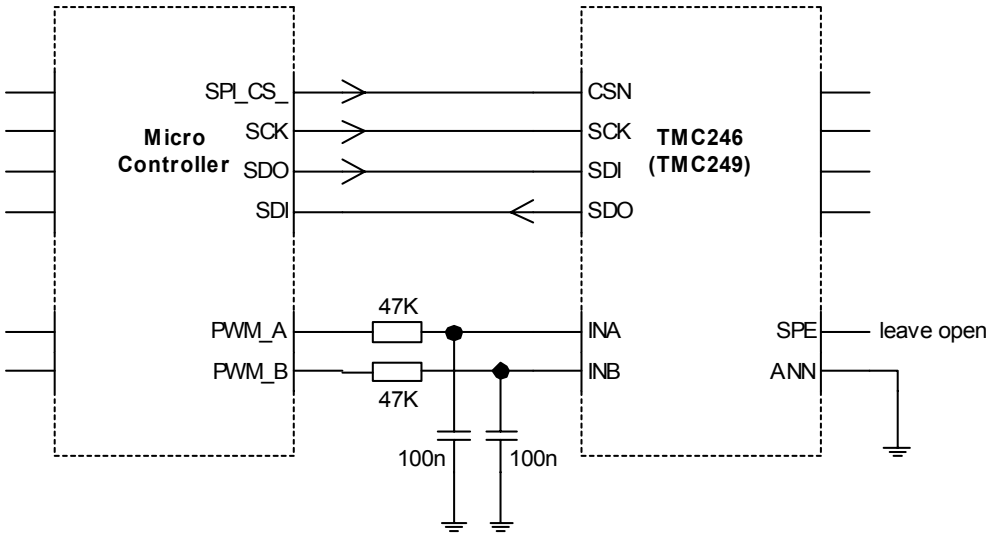
Increasing TMC246/249 Microstep Resolution in SPI-Mode

Introduction

Classical analog input controlled operation of TMC246/249 (non-SPI mode) provides very high microstep resolution limited only by the resolution of the current control input signals INA and INB. However, this non-SPI mode has the disadvantage of very poor diagnostics feedback by only one output signal (SDO=ERR pin). Furthermore, the innovative StallGuard feature of the TMC246/249 can not be utilized at all. SPI mode on the other hand supports all the diagnostic features including StallGuard but is limited to 16x microstep resolution, i.e. 16 microsteps per fullstep. With some external circuitry described at the end of the datasheet it is possible to extend microstep resolution to 64x. This application note describes a method how to increase the microstep resolution even further while still using SPI mode to benefit from StallGuard and all the diagnostic features.

Principle of Operation

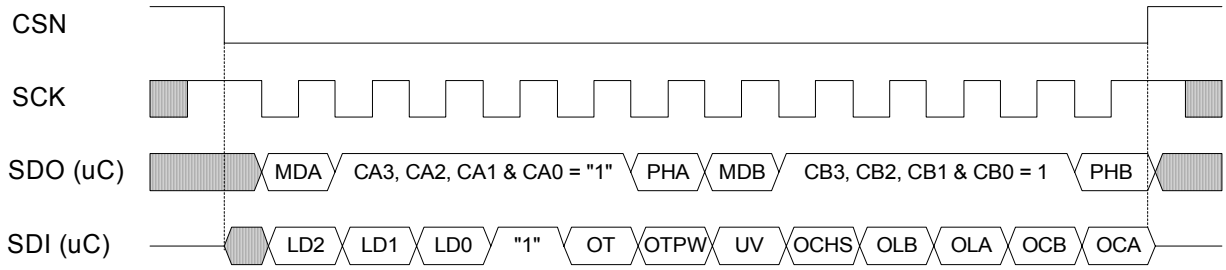
The basic idea is to combine the advantages of both the analog and the SPI mode. The phase currents of the stepper motor are controlled by the INA and INB inputs like in the analog mode while diagnostics and StallGuard information is retrieved by sending SPI datagrams. The schematic below outlines the principle:



A microcontroller with on-chip SPI hardware and two PWM channels is required. The PWM channels in conjunction with two discrete low pass filters are used to generate the pseudo-analog sinus-shaped voltages required to control the phase currents via INA and INB. ANN must be tied to GND to enable phase current control via INA and INB. The SPI on-chip hardware is used to send the phase current polarity and mixed decay control bits as well as to retrieve diagnostic information and load detection bits. SPE input should be left open to select SPI mode (internal pull-up device).

SPI Datagram

The figure below shows SPI data which has to be sent to the TMC246/249 (signal SDO) and data which is received from the TMC246/249 (signal SDI). For the meaning of the bit name abbreviations refer to the TMC246/249 datasheet.



As most microcontrollers transfer SPI data in a byte-oriented manner (i.e. in units of 8 bits) two successive bytes have to be sent (SDO) and received (SDI). The first four bits sent are don't care, the following 12 bits are interpreted as depicted above. The first 12 bits received have the meaning as depicted above, the last four bits are don't care. CSN must not go high in between the two bytes.

The mixed-decay control bits MDA and MDB can be set active ("1") while the respective phase current is decreasing to allow for faster sinusoidal current waveforms. However, MDA and MDB have to be switched off ("0") before zero crossing of the respective phase current for good load detection results (bits LD2…LD0).

The CA3…CA0 and CB3…CB0 bits all have to be "1" in all SPI datagrams ever sent to select the 100% setting of the current controlled by INA and INB inputs.

PHA and PHB have to toggled exactly during zero crossing of the respective phase current for smooth current waveforms (see "Phase Current Zero Crossing").

A new SPI datagram has to be sent only when one or more of the control bits (microcontroller SDO bits) change. As CA3…CA0 and CB3…CB0 are constant "1" all the time SPI datagrams have to be sent only when MDA/MDB or PHA/PHB change. This is the case at maximum phase current (MDA/MDB changes from "0" to "1"), short time before phase current zero crossing (MDA/MDB changes from "1" to "0") and exactly during zero crossing of the respective phase current (PHA/PHB changes from "1" to "0" or from "0" to "1"). As current zero crossing of phase A coincides with maximum current of phase B and vice versa PHA and MDB respectively PHB and MDA change at the same time. This means sending two SPI datagrams per fullstep (a quarter of an electrical period) is sufficient. With respect to the StallGuard information (load detect bits LD2…LD0) this is sufficient, too, since these are updated once per fullstep.

Phase Current Zero Crossing

While INA or INB, i.e. the duty cycle of PWM_A or PWM_B, is just zero, a SPI datagram must be send with the new polarity of the respective phase current. The rising CSN edge of this SPI datagram must occur while INA/INB is zero. Otherwise current spikes of wrong polarity in the region of the zero crossing would occur.

As an example: If PWM_A duty cycle reaches zero and PHA bit was "0" so far, then a SPI datagram has to be sent with PHA bit set to "1" and PWM_A duty cycle must still be zero when the rising CSN edge of this SPI datagram occurs.

This requires a microcontroller with fast SPI on-chip hardware to allow for proper phase current zero crossing up to high microstep rates. The maximum allowed SCK frequency of the TMC246/249 is 4 MHz, so in the best case the microcontroller should be able to do SPI transfers at 4 MHz. As an alternative one could start the SPI transfer even before INA/INB reaches zero and just generate the final rising CSN edge of the SPI transfer during the short moment of time when INA/INB is actually zero.

PWM Frequency, Duty Cycle and resulting Microstep Resolution

A PWM frequency of at least 5 KHz or higher should be appropriate to give smooth average voltages at INA/INB.

The PWM duty cycle controls the voltage level at the INA/INB input. The maximum voltage allowed for INA/INB is 3V. For maximum microstep resolution 3V should be used as the maximum value. It depends on the high voltage level of the microcontroller PWM outputs what duty cycle corresponds to 3V at INA/INB.

Two examples:

- PWM output high voltage = 5V → maximum allowed PWM duty cycle is 3V/5V = 60%
- PWM output high voltage = 3.3V → maximum allowed PWM duty cycle is 3.0V/3.3V = 91%

As one can see from these figures, the attainable microstep resolution is about 50% higher when using a supply voltage of 3.3V for the microcontroller and Vcc of TMC246/249 than that of 5V operation.

The other influencing factor on microstep resolution is the resolution of the PWM duty cycle. If this is 10 bit, i.e. 0 means 0% duty cycle and 1023 means 100% duty cycle, the resulting maximum microstepping resolution is 931 for 3.3V operation (91% of 1024) and 614 for 5V operation (60% of 1024).

Calculation of the Sense Resistor value

When operating in microstep mode (sinusoidal current waveform) the maximum allowed motor phase peak current Imax is the nominal current as specified by the motor manufacturer multiplied by 1.41 (square root of 2). The value of the sense resistor Rs depends on the desired Imax and the maximum voltage applied to INA/INB (Vref) according to the following formula:

Rs = Vref * 0.17 / Imax

Granted that Vref=3V for maximum attainable microstep resolution, this results in:

Rs = 0.51V / Imax

As an example, a phase peak current of Imax=1.5A (maximum drive current of TMC246) at a maximum reference voltage of 3V requires a sense resistor value of

Rs = 0.51V / 1.5A = 0.34 Ohms

Cascading multiple TMC246/249

It is possible to daisy-chain two or even more TMC246/249 drivers in the SDO-SDI path of the microcontroller. Simply connect SDO of the microcontroller to SDI of the first TMC246/249, SDO of the first TMC246/249 to SDI of the second TMC246/249 and so on. SDO of the last TMC246/249 has to be connected to SDI of the microcontroller. SCK and CSN respectively have to be connected in parrallel to all TMC246/249 drivers. However, two separate microcontroller PWM outputs and the corresponding external low pass filters are required for each TMC246/249 to independently control the INA/INB inputs of each

TMC246/249 driver. As an example, two daisy-chained TMC246/249 need four microcontroller PWM outputs in total.

The SPI datagrams for all daisy-chained TMC246/249 simply have to be concatenated without any de-activation of CSN in between. The first 12 bits sent and received belong to the last TMC246/249 in the chain whose SDO is connected to SDI of the microcontroller. The last 12 bits sent and received belong to the first TMC246/249 whose SDI is connected to SDO of the microcontroller.

If, for example, two TMC246/249 drivers are daisy-chained, the SPI datagram transfer would comprise 24 bits, i.e. three bytes in total.